(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 January 2001 (25.01.2001)

PCT

(10) International Publication Number
WO 01/06565 A1

(51) International Patent Classification[7]: H01L 27/142

(21) International Application Number: PCT/US00/07403

(22) International Filing Date: 20 March 2000 (20.03.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/353,526 14 July 1999 (14.07.1999) US

(71) Applicant: HUGHES ELECTRONICS CORPORATION [US/US]; 200 North Sepulveda Boulevard, El Segundo, CA 90245 (US).

(72) Inventors: BOUTROS, Karim, S.; 11976 Bubbling Brook Street, Moorpark, CA 93021 (US). KRUT, Dmitri, D.; 17110 Clemons Drive, Encino, CA 91436 (US). KARAM, Nasser, H.; 10314 Saddlewood Lane, Northridge, CA 91326 (US).

(74) Agents: DURAISWAMY, Vijayalakshmi, D. et al.; Hughes Electronics Corporation, Bldg. 001, MS A109, P.O. Box 956, El Segundo, CA 90245 (US).

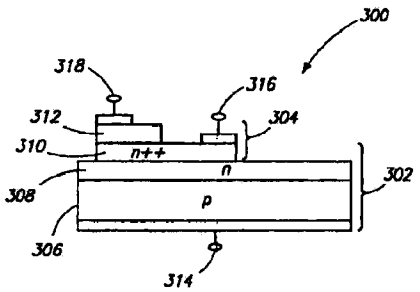
(81) Designated State *(national)*: JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

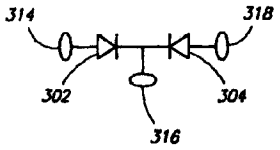
Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: MONOLITHIC BYPASS-DIODE AND SOLAR-CELL STRING ASSEMBLY



A



B

(57) Abstract: An apparatus and method for making a solar cell with an integrated bypass diode. The method comprises the steps of depositing a second layer having a first type of dopant on a first layer having an opposite type of dopant to the first type of dopant to form a solar cell, depositing a third layer having the first type of dopant on the second layer, depositing a fourth layer having the opposite type of dopant on the third layer, the third layer and fourth layer forming a bypass diode, selectively etching the third layer and the fourth layer to expose the second layer and the third layer, and applying contacts to the fourth layer, third layer, and the first layer to allow electrical connections to the assembly. The apparatus comprises a first layer having a first type of dopant, a second layer having a second type of dopant opposite to the first type of dopant, wherein the first layer and the second layer form a solar cell, a third layer, coupled to the second layer, and a fourth layer, coupled to the third layer, the third layer and the fourth layer forming a bypass diode.

WO 01/06565 A1

MONOLITHIC BYPASS-DIODE AND SOLAR-CELL STRING ASSEMBLY

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to devices and methods for making semiconductor devices, and in particular to a device and method for making monolithic bypass-diodes and solar-cell string assemblies.

2. Description of the Related Art.

Solar cells are used in various technologies to provide power to other electronic assemblies. Satellites, calculators, and power systems are all examples of solar cell usage.

A solar cell is a p-n junction created over a large area on a semiconductor substrate. Solar cells are typically long-life devices, but can have their efficiency reduced or destroyed by reverse biasing of the solar cell junction. To prevent this type of damage, bypass diodes (BDs) are used to allow current to flow in an anti-parallel direction to the current flow through the solar cell junction.

Bypass diodes are typically formed using an isolated island structure and/or created in a recess of the back (reverse) of the solar cell substrate, and connected to the solar cell using additional wiring and/or additional metallization on the solar cell substrate. The use of additional wiring and/or additional metallization creates new failure points for solar cells, as well as adding to the weight and complexity of the solar cell structure. Additional weight and failure mechanisms are unacceptable in a spacecraft environment, because of the extreme additional costs involved. Further, additional metallization obscures the solar cell from receiving incident light, which reduces the efficiency of the solar cell structure.

FIGS. 1A-1B illustrate a related art device that integrates bypass diodes with solar cells.

FIG. 1A illustrates a cross-sectional view of a semiconductor device. Assembly 100 comprises solar cell 102 and bypass diode 104. Solar cell 102 utilizes an n-doped substrate 106 and a coupled p-doped layer 108. Substrate 106 and layer 108 are coupled electrically, such that a depletion layer is created between substrate 106 and layer 108. The method of coupling can be, for example, deposition of layer 108 on substrate 106, diffusion of p-type carriers into substrate 106 to form layer 108, chemical vapor deposition of layer 108, epitaxial growth of layer 108 on substrate 106, or other methods.

Bypass diode 104 utilizes a p-doped layer 110 and an n-doped layer 112 to create a separate p-n junction. Layer 110 is electrically coupled to substrate 106, and is isolated from layer 108 by a dielectric isolation layer 114. External connections 116 and 118 are complemented by metallization connections 120 and 122 to create the solar cell/bypass diode assembly 100. A more extensive description of the device illustrated in FIG. 1A can be found in U.S. Patent No. 4,759,803, issued July 26, 1988, which is herein incorporated by reference.

FIG. 1B illustrates a schematic diagram for assembly 100. Bypass diode 104 and solar cell 102 are connected in an anti-parallel configuration, with external connections 116 and 118 shown, in order to connect the assembly 100 to other assemblies 100.

The limitations of the assembly 100 shown in FIG. 1A is that there is a third p-n junction in the assembly, namely, that created by the coupling of layer 110 and substrate 106. Further, the active area of the solar cell 102, shown as area 124, is reduced by the

physical size of isolation layer 114 and the presence of bypass diode 104. Since the active area 124 of the solar cell is smaller than without bypass diode 104, a larger number of solar cells 102 will be required to produce a given amount of power. The assembly also uses a large metallization area, namely 120 and 122, which makes processing the assembly 100 more difficult, and reduces the yield because of the failures of the interconnections 120 and 122.

It can be seen that there is a need in the art for a solar cell that has an integrated bypass diode. It can also be seen that there is a need in the art for a solar cell that has a bypass diode that minimizes the need for additional wiring and/or metallization interconnects. It can also be seen that there is a need in the art for a bypass diode that minimizes the weight and failure points for solar cell devices.

SUMMARY OF THE INVENTION

To address the requirements described above, the present invention discloses a method, and apparatus for providing a bypass diode and solar cell string assembly. The assembly is monolithic and uses standardized semiconductor processing techniques to produce a bypass diode on the solar cell substrate.

The method comprises the steps of depositing a second layer having a first type of dopant on a first layer having an opposite type of dopant to the first type of dopant to form a solar cell, depositing a third layer having the first type of dopant on the second layer, depositing a fourth layer having the opposite type of dopant on the third layer, the third layer and fourth layer forming a bypass diode, selectively etching the third layer and the fourth layer to expose the second layer and the third layer, and applying contacts to the fourth layer, third layer, and the first layer to allow electrical connections to the assembly.

The apparatus comprises a first layer having a first type of dopant, a second layer having a second type of dopant opposite to the first type of dopant, wherein the first layer and the second layer form a solar cell, a third layer, coupled to the second layer, and a fourth layer, coupled to the third layer, the third layer and the fourth layer forming a bypass diode.

The present invention provides a solar cell that has an integrated bypass diode. The present invention also provides a solar cell that has a bypass diode that minimizes the need for additional wiring and/or metallization interconnects, as well as minimizing the weight and failure points for solar cell devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIGS. 1A-1B illustrate a related art device that integrates bypass diodes with solar cells;

FIGS. 2A-2B illustrate a device in accordance with the present invention that integrates bypass diodes with solar cells;

FIGS. 3A-3B illustrate an alternative embodiment and alternative schematic of the solar cell assembly of the present invention;

FIGS. 4A-4B illustrate an alternative embodiment and alternative schematic of the solar cell assembly of the present invention;

FIG. 5 illustrates a connection strategy for the devices made as described in FIGS. 3A and 4A;

FIG. 6 illustrates the interconnection schema required by the related art;

FIG. 7 illustrates the interconnection schema used by the present invention;

FIG. 8 illustrates a completed structure in accordance with the present invention;

FIG. 9 illustrates a schematic for the structure described in FIG. 8; and

FIG. 10 is a flow chart showing the operations used to practice one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, reference is made to the accompanying drawings which form a part hereof, and which is shown, by way of illustration, several embodiments of the present invention. It is understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Overview

The present invention monolithically incorporates a bypass diode into a solar cell assembly. The present invention creates the bypass diode without complex processing steps, which increases the yield for the finished device.

Related art processes, such as those described in U. S. Patent No. 5,616,185, entitled "SOLAR CELL WITH INTEGRATED BYPASS DIODE AND METHOD," describe using a discrete bypass diode that is integrated with the solar cell as a hybrid assembly. The bypass diode is integrated with the solar cell by forming recesses on the non-illuminated side of the solar cell and placing at least one discrete low-profile bypass diode in the recesses so that each bypass diode is approximately flush with the back side of the solar cell. Each bypass diode is then bonded to the solar cell for anti-parallel connection across the solar cell.

The back side of the solar cell is preferably formed with a honeycomb pattern of recesses to reduce the weight of the solar cell while maintaining mechanical strength. The recesses that receive bypass diodes preferably have a rectangular shape that better accommodates the bypass diode.

This related art technique makes the solar cell difficult to make, because the rear of the solar cell must be patterned and etched to receive the bypass diodes, and the bypass diodes must then be electrically connected to the solar cells. These additional process steps are costly and provide additional failure mechanisms for the completed assembly.

FIGS. 2A-2B illustrate a device in accordance with the present invention that integrates bypass diodes with solar cells.

FIG. 2A shows assembly 200, comprising solar cell 202 and bypass diode 204. Solar cell 202 utilizes an p-doped substrate 206 and a coupled n-doped layer 208.

Although substrate 206 is shown as a wafer, substrate 206 can be a dopant well within a wafer, an isolated structure on top of a wafer, a layer or other structure, and is not limited to the wafer structure illustrated in FIG. 2A. Further, solar cell 202, although shown as a single junction cell, can be a two junction solar cell 202, a three junction solar cell 202, or an n-junction solar cell 202, where n is any number. The present invention is not limited to single junction solar cells 202.

Substrate 206 and layer 208 are coupled electrically, such that a depletion layer is created between substrate 206 and layer 208. The method of coupling can be, for example, deposition of layer 208 on substrate 206, diffusion of n-type carriers into substrate 206 to form layer 208, chemical vapor deposition of layer 208, epitaxial growth of layer 208 on substrate 206, or other methods. Substrate 206 is typically germanium, but can comprise other materials such as silicon, indium phosphide (InP), gallium arsenide (GaAs), gallium phosphide (GaP), gallium indium phosphide (GaInP), or other materials.

Bypass diode 204 comprises a multilayer diode structure, having layers 210-216. Layer 210 is a highly n-doped (n++) layer, and is coupled to layer 208. Layer 212 is a highly p-doped (p++) layer, layer 214 is a p-doped layer, and layer 216 is an n-doped layer. Layer 210 is used as a tunnel junction to connect to contact 218. Layers 214 and 216 create a p-n junction, and comprise the bypass diode 204. Although a single bypass diode 204 is shown, the present invention envisions multiple bypass diodes 204 manufactured for a given solar cell 202. Multiple bypass diodes 204 provide redundancy for a solar cell 202. Bypass diode 204 is typically gallium arsenide or a III-V semiconductor structure, such as alloys of gallium, indium, and aluminum with arsenic, phosphorous, and antimony, but can also be silicon, germanium, combinations of silicon and germanium with or without carbon, II-VI semiconductor materials, other ternary or quaternary combinations of semiconductor materials, or other materials.

Electrical contact 220 is coupled to substrate 206, and electrical interconnect 222 is deposited on isolation layer 224 such that electrical interconnect 222 couples layer 216 with substrate 206. Substrate 206 has a low electrical resistivity, and, as such, electrical interconnect 222 is effectively coupled to the electrical contact 220 on the bottom (back) of substrate 206. Alternatively, electrical interconnect 222 can be formed using a wrap-

around tab contact to connect layer 216 to substrate 206. Isolation layer 224 can be formed by hard dielectrics, such as oxides and nitrides, or by soft dielectrics, such as polyimides, or other methods.

The layers 208-216, contacts 218-220, and interconnect 222 are defined lithographically and etched using any standard etching method to determine the geometric shapes desired for each of the elements of the assembly 200. Although not shown, additional layers can be used to assist in the photolithographic and/or manufacturing processes, such as stop etch layers, etc., which are additional layers within the assembly 200 that control the etching of specific areas of the assembly 200.

Active area 226 for solar cell 202, as compared to area 124, is now much larger, which results in a solar cell 202 that can generate more power for a given area. Further, the assembly 200 can be made using standard fabrication techniques, and does not require etching or other removal of material from the back of the solar cell 202 to install hybrid discrete bypass diodes 204. Although discussed with respect to a p-doped substrate 206, an n-doped substrate 206, with appropriately doped layers 208-214, can also be used in accordance with the present invention.

FIG. 2B illustrates a schematic diagram for assembly 200. Bypass diode 204 and solar cell 202 are connected in an anti-parallel configuration, with external connections 218 and 220 shown, in order to connect the assembly 200 to other assemblies 200.

FIGS. 3A-3B illustrate an alternative embodiment and alternative schematic of the solar cell assembly of the present invention.

FIG. 3A shows assembly 300, comprising solar cell 302 and bypass diode 304. Solar cell 302 utilizes an p-doped substrate 306 and a coupled n-doped layer 308. Substrate 306 and layer 308 are coupled electrically, such that a depletion layer is created between substrate 306 and layer 308. The method of coupling can be, for example, deposition of layer 308 on substrate 306, diffusion of n-type carriers into substrate 306 to form layer 308, chemical vapor deposition of layer 308, epitaxial growth of layer 308 on substrate 306, or other methods. Substrate 306 is typically germanium, but can comprise other materials such as silicon, indium phosphide (InP), gallium arsenide (GaAs), gallium phosphide (GaP), gallium indium phosphide (GaInP), or other materials.

Although substrate 306 is shown as a wafer, substrate 306 can be a dopant well within a wafer, an isolated structure on top of a wafer, a layer or other structure, and is not limited to the wafer structure illustrated in FIG. 3A. Further, solar cell 302, although shown as a single junction cell, can be a two junction solar cell 302, a three junction solar cell 302, or an n-junction solar cell 302, where n is any number. The present invention is not limited to single junction solar cells 302.

Bypass diode 304 comprises layers 310-312. Layer 310 is a highly n-doped (n++) layer, and is coupled to layer 308. Layer 312 is a p-doped layer and is coupled to layer 310. Although a single bypass diode 304 is shown, the present invention envisions multiple bypass diodes 304 manufactured for a given solar cell 302. Multiple bypass diodes 304 provide redundancy for a solar cell 302. Bypass diode 304 is typically gallium arsenide or a III-V semiconductor structure such as alloys of gallium, indium, and aluminum with arsenic, phosphorous, and antimony, but can also be silicon, germanium, combinations of silicon and germanium with or without carbon, II-VI semiconductor materials, ternary or quaternary combinations of semiconductor materials, or other materials.

The structure of assembly 300 contains three contacts, namely contacts 314-318. Assembly 300 now only involves the deposition of a single layer, namely layer 312, to create the bypass diode 304. Etching and photolithographical techniques then define the layers 306-312 for proper attachment of the contacts 314-318. The simpler processing steps used to create the assembly 300 of the present invention increases the yield for the devices, and also reduces costs during the production run for assembly 300. Although not shown, additional layers can be used to assist in the photolithographic and/or manufacturing processes, such as stop etch layers, etc., which are additional layers within the assembly 300 that control the etching of specific areas of the assembly 300. Although discussed with respect to a p-doped substrate 306, an n-doped substrate 306, with appropriately doped layers 308-312, can also be used in accordance with the present invention.

FIG. 3B is a schematic diagram for the assembly 300 illustrated in FIG. 3A. Since there are now three contacts 314-318, solar cell 302 and bypass diode 304 are no longer connected in an anti-parallel technique as in the assemblies 100 and 200.

However, bypass diode 304 for a given solar cell 302 is connected to a solar cell of a different assembly 300 to create the anti-parallel connections required to provide the reverse bias protection for the assembly 300. The connection for such a structure is discussed with respect to FIG. 5.

FIGS. 4A-4B illustrate an alternative embodiment and alternative schematic of the solar cell assembly of the present invention.

FIG. 4A shows assembly 400, comprising solar cell 402 and bypass diode 404. Solar cell 402 utilizes an p-doped substrate 406 and a coupled n-doped layer 408. Substrate 406 and layer 408 are coupled electrically, such that a depletion layer is created between substrate 406 and layer 408. The method of coupling can be, for example, deposition of layer 408 on substrate 406, diffusion of n-type carriers into substrate 406 to form layer 408, chemical vapor deposition of layer 408, epitaxial growth of layer 408 on substrate 406, or other methods. Substrate 406 is typically germanium, but can comprise other materials such as silicon, indium phosphide (InP), gallium arsenide (GaAs), gallium phosphide (GaP), gallium indium phosphide (GaInP), or other materials.

Although substrate 406 is shown as a wafer, substrate 406 can be a dopant well within a wafer, an isolated structure on top of a wafer, a layer or other structure, and is not limited to the wafer structure illustrated in FIG. 4A. Further, solar cell 402, although shown as a single junction cell, can be a two junction solar cell 402, a three junction solar cell 402, or an n-junction solar cell 402, where n is any number. The present invention is not limited to single junction solar cells 402.

Bypass diode 404 comprises layers 410-414. Layer 410 is a highly n-doped (n++) layer, and is coupled to layer 408. Layer 412 is an n-doped layer and is coupled to layer 310, and layer 414 is an p-doped layer and is coupled to layer 412. Layers 412-414 create a p-n junction, and comprise the bypass diode 404. Bypass diode 404 is typically gallium arsenide or a III-V semiconductor structure such as alloys of gallium, indium, and aluminum with arsenic, phosphorous, and antimony, but can also be silicon, germanium, combinations of silicon and germanium with or without carbon, II-VI semiconductor materials, ternary or quaternary combinations of semiconductor materials, or other materials.

The structure of assembly 400 contains three contacts, namely contacts 416-420. Assembly 400 now only involves the deposition of a two additional layers, namely layers 412 and 414, to create the bypass diode 404. Etching and photolithographical techniques then define the layers 406-414 for proper attachment of the contacts 416-420. The simpler processing steps used to create the assembly 400 of the present invention increases the yield for the devices, and also reduces costs during the production run for assembly 300. Layer 414 contains a lower dopant density (p instead of p++) to provide a lower leakage current in the bypass diode 404, which increases the efficiency of the overall assembly 400. Although discussed with respect to a p-doped substrate 406, an n-doped substrate 406, with appropriately doped layers 408-414, can also be used in accordance with the present invention.

FIG. 4B is a schematic diagram for the assembly 400 illustrated in FIG. 3A. Since there are now three contacts 416-420, solar cell 402 and bypass diode 404 are no longer connected in an anti-parallel technique as in the assemblies 100 and 200. However, bypass diode 404 for a given solar cell 402 is connected to a solar cell of a different assembly 400 to create the anti-parallel connections required to provide the reverse bias protection for the assembly 400. The connection for such a structure is discussed with respect to FIG. 5.

FIG. 5 illustrates a connection strategy for the devices made as described in FIGS. 3A and 4A. A series of a number (i) assemblies 400, or alternatively, 300, are connected as shown in FIG. 5. Each assembly 400 is numbered, e.g., 1, 2, ... i. The contact 418 of the first assembly is coupled to contact 416 of the second assembly 400, which electrically connects the cathode of solar cell 402 and the anode of bypass diode 404 of the first assembly 400 to the anode of solar cell 402 of the second assembly. This approach allows for a ladder-like connection of the solar cells 402 and the bypass diodes 404 for all of the assemblies 400, such that each bypass diode 404 protects the solar cell 402 of the assembly 400 adjacent. Further, the first assembly 400 and the ith assembly 400 can be connected as shown in FIG. 5, such that the ith bypass diode 404 protects the first solar cell 402. If desired, the ith bypass diode 404 can also protect a different solar cell 402, e.g., a solar cell 402 in a different series string of assemblies 400. The interconnect schema shown in FIG. 5 provides protection for each solar cell 400 in the

string of solar cells 402. This type of interconnection, along with the assembly structure shown in FIGS. 3A and 4A, eliminates the isolation requirement within each assembly 300 and 400, thus decreasing the complexity of the manufacture of the assemblies 300 and 400.

FIG. 6 illustrates the interconnection schema required by the related art.

Solar cells 600 and bypass diodes 602 are physically connected by mounting bypass diodes 602 on the rear (non-illuminated) portion of solar cells 600. String connection 604 couples one solar cell 600 to another solar cell 600, which places solar cells 600 in a series connection to produced a desired output voltage from solar cells 600. To connect bypass diode 602 to solar cell 600, solder contact 604 and wrap-around connection 606 must be used to electrically connect the bypass diode 604 to the solar cell 600. Further, to properly form wrap-around connection 606, insulator 608 must be positioned to prevent electrical shorting between the layers within solar cell 600 and the layers of bypass diode 602. Additional information regarding the solar cells 600 and bypass diodes 602 shown in FIG. 6 can be found in commonly assigned U.S. Patent No. 5,616,185, issued April 1, 1997, which is hereby incorporated by reference.

FIG. 7 illustrates the interconnection schema used by the present invention. The embodiment of the present invention shown in FIG. 2 does not require the bypass diode to be connected externally to the solar cell, since metallization on the assembly connects the bypass diode to the solar cell properly. For the embodiments of the present invention shown in FIGS. 3 and 4, solar cell 700 and bypass diode 702 are connected using contact 704. String connection 706 is again used to series connect one solar cell 700 to another solar cell 700 to produce the proper voltage for the string. The present invention eliminates the need for solder connections between the bypass diode 702 and the solar cell 700, as well as the insulator and wrap-around connection required by the related art. The elimination of these elements makes the assembly easier to produce and integrate into a final assembly.

FIG. 8 illustrates a completed structure in accordance with the present invention. Assembly 800 comprises substrate 802, solar cell 804, solar cell 806, isolation layer 808, bypass diode 810, and contact layer 812. Isolation layer 814 and contacts 816-820

complete the structure. Dice line 822 is created to separate assembly 800 from other assemblies 800 on substrate 802.

The solar cells 804 and 806 are shown as being formed of different materials, e.g., solar cell 804 is formed out of GaAs, whereas solar cell 806 is formed out of GaInP. However, solar cells 804 and 806 can be formed of the same materials, or other materials than shown in FIG. 8, without departing from the scope of the present invention. Further, the isolation layer 808 is not required, as discussed with respect to FIG. 3A.

Although bypass diode 810 can be formed anywhere on the assembly 800, placing bypass diode 810 near the edge of the cell, e.g., near dice line 822, simplifies the assembly 800 contact 816-820 formation.

FIG. 9 illustrates a schematic for the structure described in FIG. 8. As shown, bypass diode 810 is connected in an anti-parallel configuration with the series connection of solar cells 804 and 806.

Process Chart

FIG. 10 is a flow chart showing the operations used to practice one embodiment of the present invention.

Block 1000 represents performing the step of depositing a second layer having a first type of dopant on a first layer having an opposite type of dopant to the first type of dopant to form a solar cell.

Block 1002 represents performing the step of depositing a third layer having the first type of dopant on the second layer.

Block 1004 represents performing the step of depositing a fourth layer having the opposite type of dopant on the third layer, the third layer and fourth layer forming a bypass diode.

Block 1006 represents performing the step of selectively etching the third layer and the fourth layer to expose the second layer and the third layer.

Block 1008 represents performing the step of applying contacts to the fourth layer, third layer, and the first layer to allow electrical connections to the assembly.

Conclusion

This concludes the description of the preferred embodiments of the present invention. In summary, the present invention describes an apparatus and method for making a monolithic bypass diode and solar cell assembly. Although described herein using a single junction solar cell, the present invention can be used with solar cells having any number of junctions. The method comprises the steps of depositing a second layer having a first type of dopant on a first layer having an opposite type of dopant to the first type of dopant to form a solar cell, depositing a third layer having the first type of dopant on the second layer, depositing a fourth layer having the opposite type of dopant on the third layer, the third layer and fourth layer forming a bypass diode, selectively etching the third layer and the fourth layer to expose the second layer and the third layer, and applying contacts to the fourth layer, third layer, and the first layer to allow electrical connections to the assembly. The apparatus comprises a first layer having a first type of dopant, a second layer having a second type of dopant opposite to the first type of dopant, wherein the first layer and the second layer form a solar cell, a third layer, coupled to the second layer, and a fourth layer, coupled to the third layer, the third layer and the fourth layer forming a bypass diode.

The foregoing description of the preferred embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. For example, the bypass diode can be placed under the contact pad of the solar cell instead of in a separate mesa structure as illustrated. Further, some or all of the contacts between the solar cell and the bypass diode can be made using external or mechanical means instead of metallization steps. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is Claimed is:

1. A solar cell assembly, comprising:

a first layer having a first type of dopant;

a second layer having a second type of dopant opposite to the first type of dopant, the second layer coupled to the first layer, the first layer and the second layer forming a solar cell;

a third layer, coupled to the second layer; and

a fourth layer, coupled to the third layer, the third layer and fourth layer forming a bypass diode.

2. The assembly of claim 1, wherein the bypass diode of a first assembly is connected in anti-parallel with the solar cell of a second assembly.

3. The assembly of claim 1, further comprising a fifth layer disposed between the third layer and the fourth layer, wherein the fourth layer and the fifth layer form a bypass diode.

4. The assembly of claim 3, wherein the bypass diode of a first assembly is connected with the solar cell of a second assembly in an anti-parallel configuration.

5. An solar cell assembly with an integrated bypass diode, comprising:

a solar cell, comprising a first layer having a first dopant type and a second layer having a dopant type opposite to the first dopant type;

a tunnel junction layer, coupled to the solar cell; and

a bypass diode, coupled to the tunnel junction layer, comprising a third layer having the first dopant type and a fourth layer having the opposite dopant type, the fourth layer being electrically coupled to the first layer for creating an anti-parallel configuration of the solar cell and the bypass diode therein.

6. The solar cell assembly of Claim 5, further comprising a second solar cell disposed between the solar cell and the tunnel junction layer.

7. A method for making a solar cell and an integrated bypass diode assembly, comprising the steps of:

depositing a first layer having a first type of dopant on a second layer having an opposite type of dopant to the first type of dopant to form a solar cell;

depositing a third layer having the first type of dopant on the first layer;

depositing a fourth layer having the opposite type of dopant on the third layer, the third layer and the fourth layer forming a bypass diode;

selectively etching the third layer and the fourth layer to expose the first layer and the third layer; and

applying contacts to the second layer, the third layer, and the fourth layer to allow electrical connections to the assembly.

8. The method of claim 7, further comprising the steps of:

connecting the contact on the substrate of a first assembly to the contact on the second layer of a second assembly; and

connecting the contact on the second layer of the first assembly to the contact on the third layer of the second assembly for connecting the solar cell of the first assembly to the bypass diode of the second assembly in an anti-parallel configuration.

9. The method of claim 7, further comprising the step of depositing a fourth layer disposed between the second layer and third layer, wherein the third layer and the fourth layer form a bypass diode.

10. The method of claim 7, further comprising the step of depositing a fourth layer and a fifth layer disposed between the substrate and the first layer, wherein the substrate and the fourth layer form a first solar cell and the fifth layer and the first layer form a second solar cell.

11. A solar cell assembly, comprising:

a first layer having a first type of dopant;

a second layer having a second type of dopant opposite to the first type of dopant, the second layer coupled to the first layer, the first layer and the second layer forming a first solar cell junction;

a third layer, coupled to the second layer;

a fourth layer, coupled to the third layer, the third layer and fourth layer forming a second solar cell junction, the first solar cell junction and the second solar cell junction forming a solar cell;

a fifth layer, coupled to the fourth layer; and

a sixth layer, coupled to the fifth layer, the fifth layer and the sixth layer forming a bypass diode.

12. The assembly of claim 11, wherein the bypass diode of a first assembly is connected in anti-parallel with the solar cell of a second assembly.

13. A solar cell assembly, comprising:

a first layer having a first type of dopant;

a second layer having a second type of dopant opposite to the first type of dopant, the second layer coupled to the first layer, the first layer and the second layer forming a first solar cell junction;

a third layer, coupled to the second layer;

a fourth layer, coupled to the third layer, the third layer and fourth layer forming a second solar cell junction;

a fifth layer, coupled to the fourth layer;

a sixth layer, coupled to the fifth layer, the fifth layer and the sixth layer forming a third solar cell junction, the first solar cell junction, the second solar cell junction, and the third solar cell junction forming a solar cell;

a seventh layer, coupled to the sixth layer; and

an eighth layer, coupled to the seventh layer, the seventh layer and the eighth layer forming a bypass diode.

14. The assembly of claim 13, wherein the bypass diode of a first assembly is connected in anti-parallel with the solar cell of a second assembly.

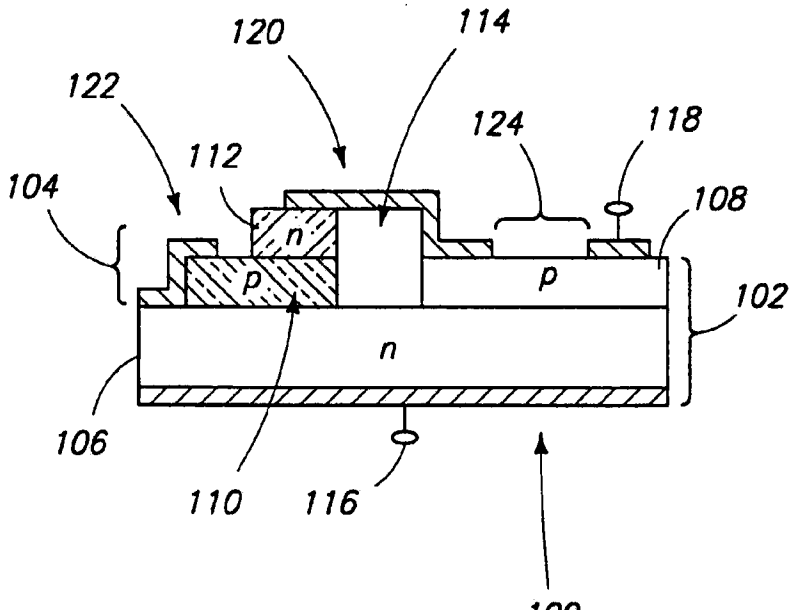

120
114
122
124
118
112
104
108
n
p
p
102
n
106
110
116
100

FIG. 1A

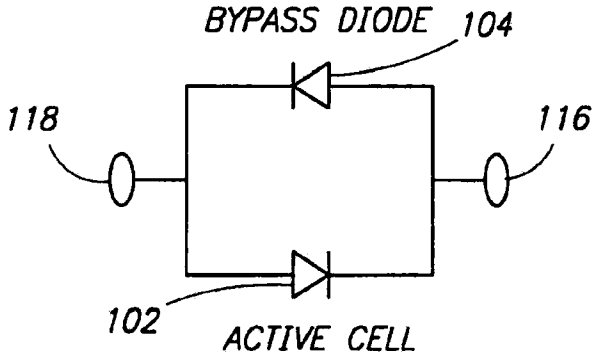

BYPASS DIODE
104
118
116
102
ACTIVE CELL

FIG. 1B

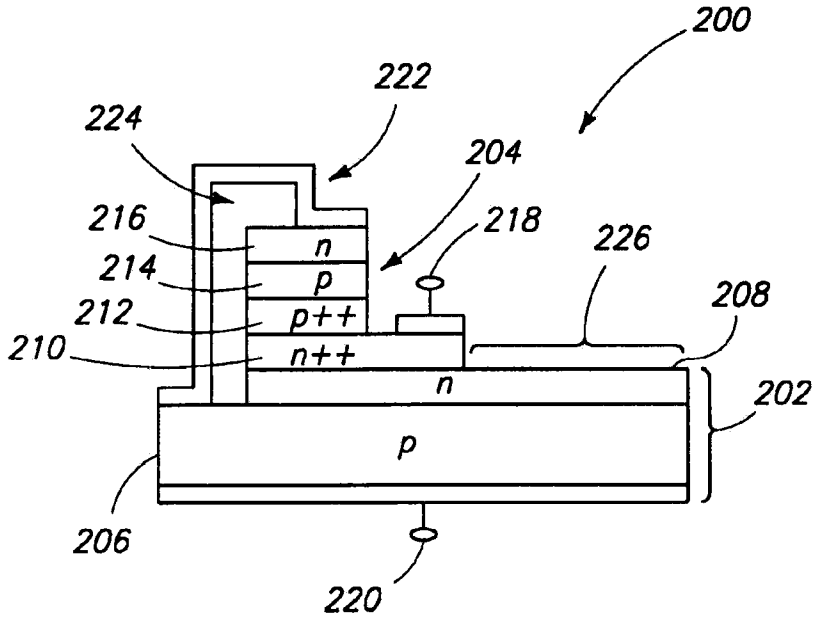

200
222
224
204
216
218
226
214
208
212
210
202
206
220
n
p
p++
n++
n
p

FIG. 2A

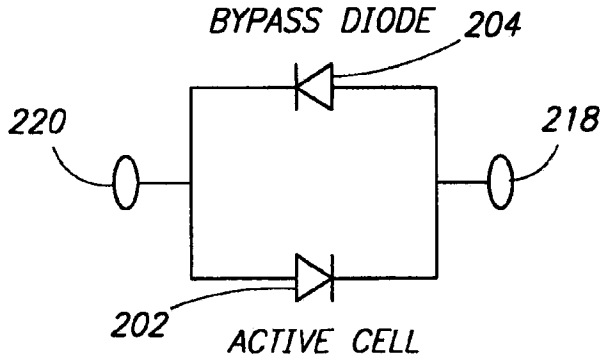

BYPASS DIODE
204
220
218
202
ACTIVE CELL

FIG. 2B

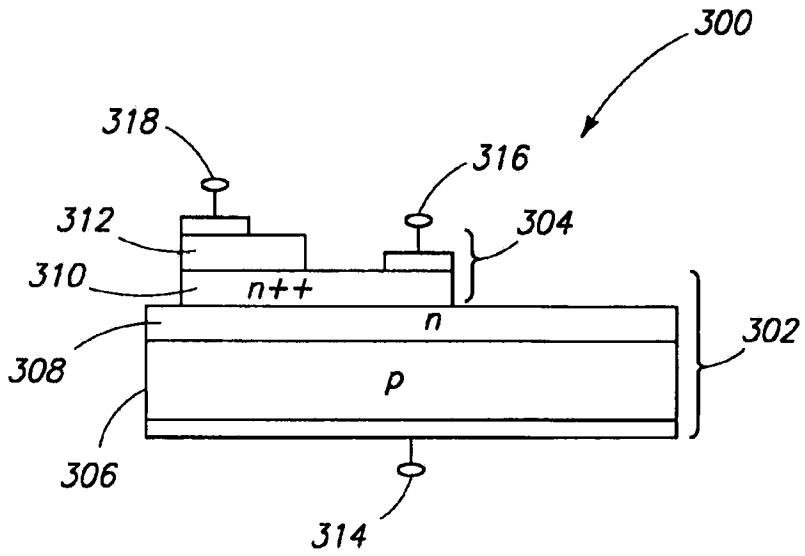


FIG. 3A

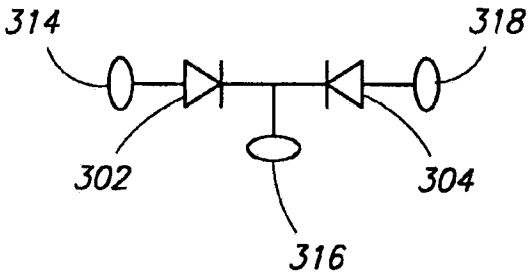


FIG. 3B

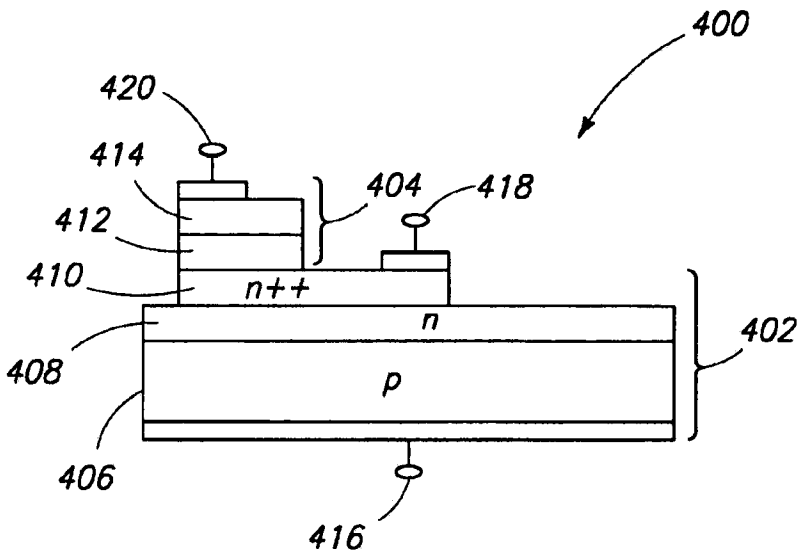

400
420
414
404
418
412
410
n++
n
402
408
p
406
416

FIG. 4A

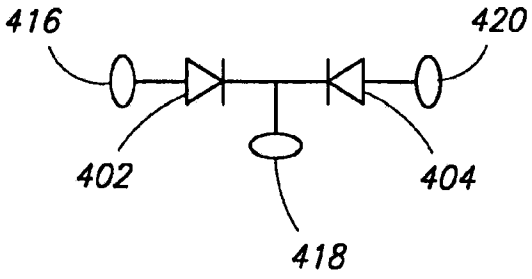

416
420
402
404
418

FIG. 4B

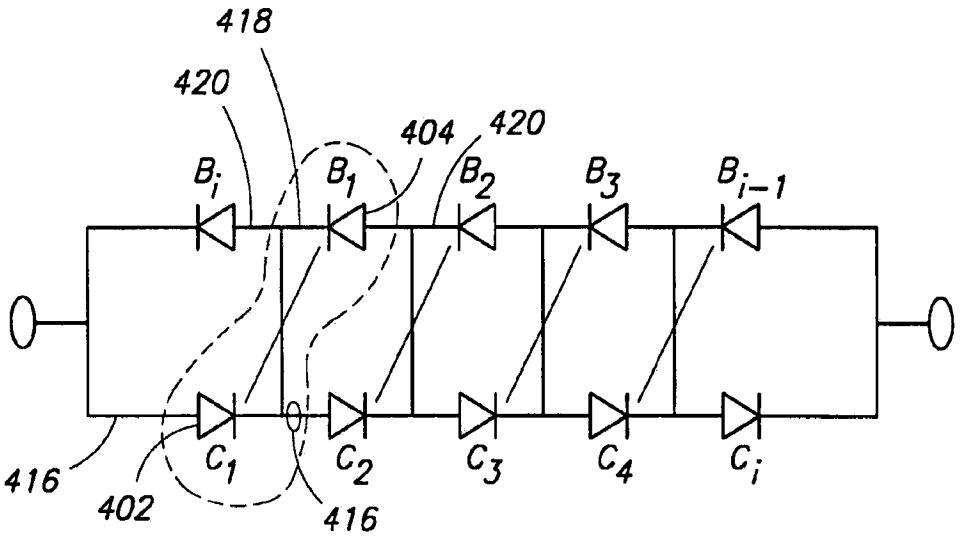

418
420
404
420
B_i
B_1
B_2
B_3
B_{i-1}
C_1
C_2
C_3
C_4
C_i
416
402
416

FIG. 5

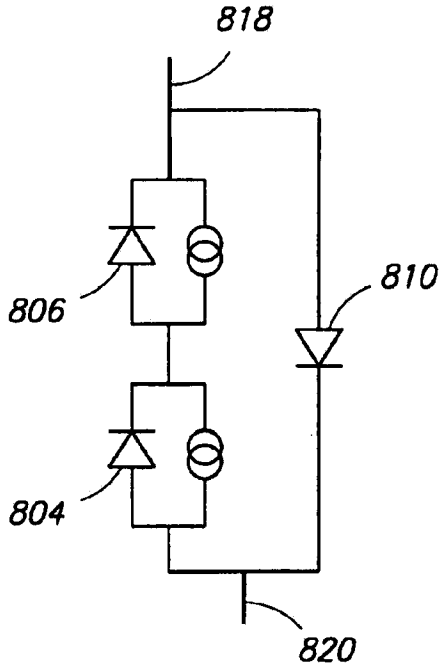

818
806
810
804
820

FIG. 9

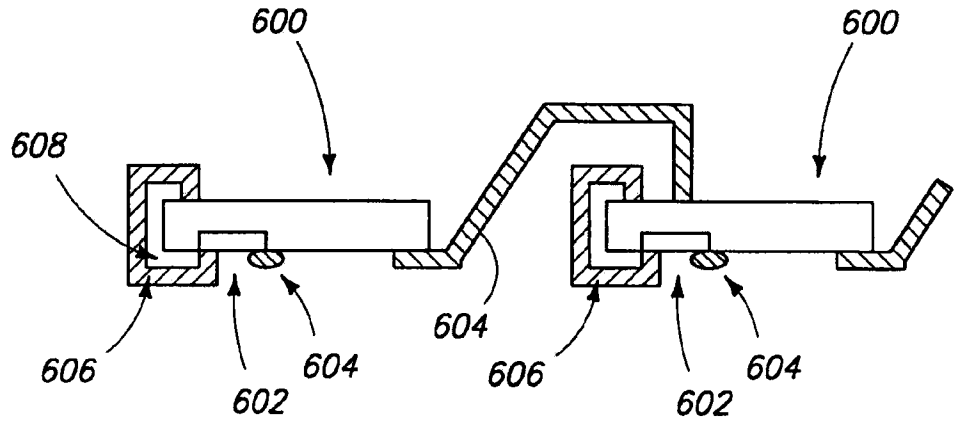


FIG. 6

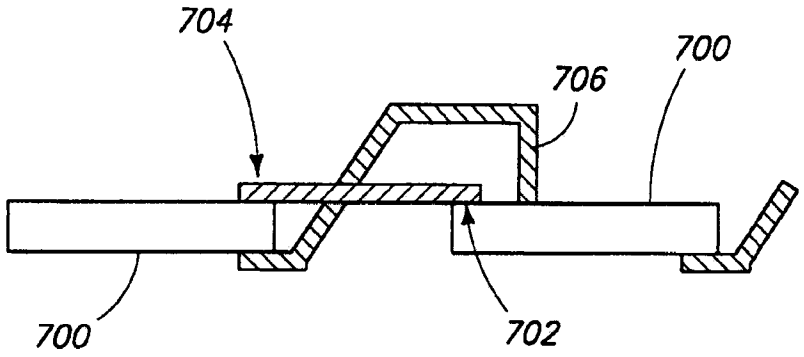


FIG. 7

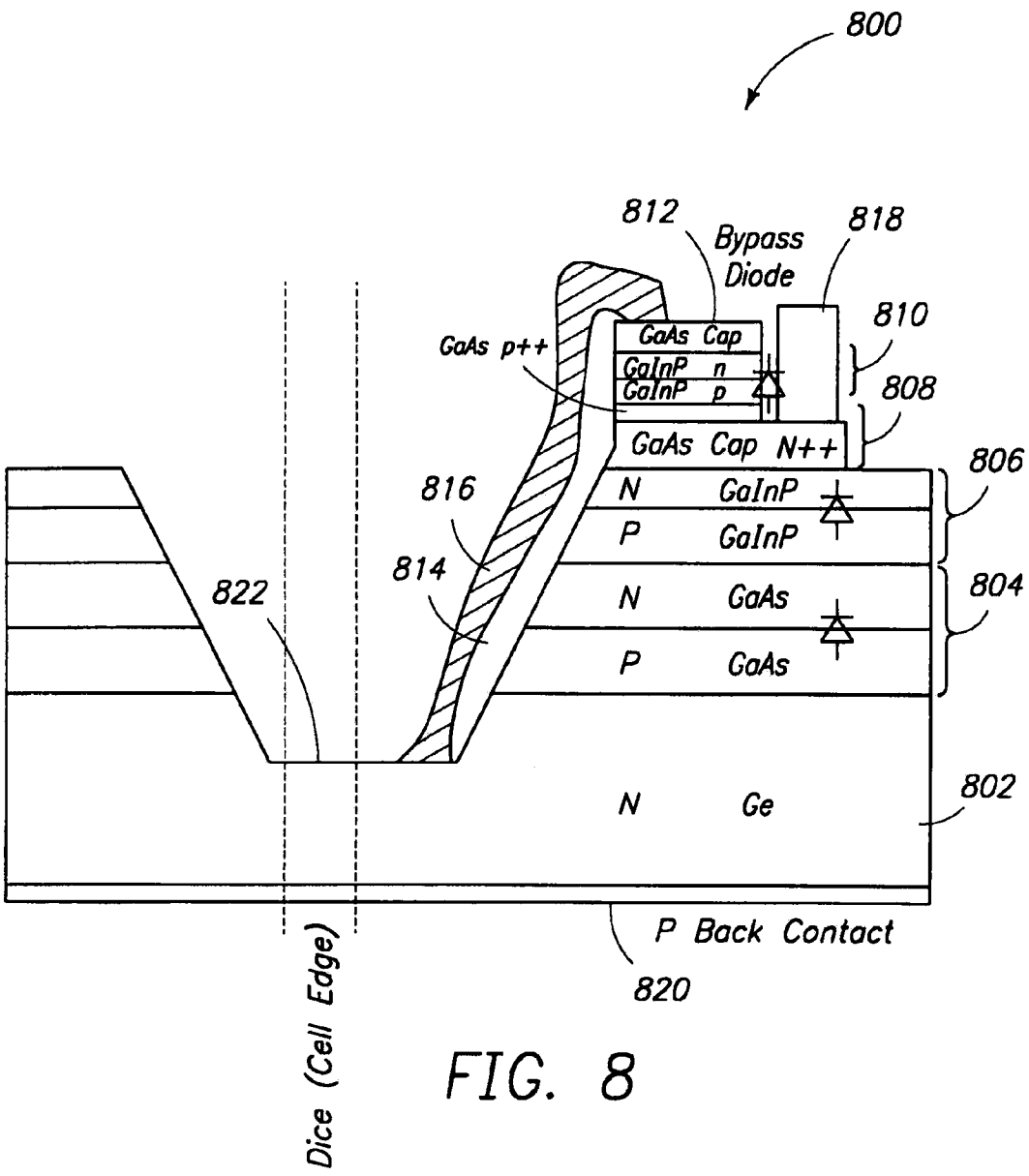

800
812
Bypass
Diode
818
810
808
GaAs p++
GaAs Cap
GaInP n
GaInP p
GaAs Cap N++
806
816
814
822
N GaInP
P GaInP
N GaAs
P GaAs
804
N Ge
802
P Back Contact
820
Dice (Cell Edge)

FIG. 8

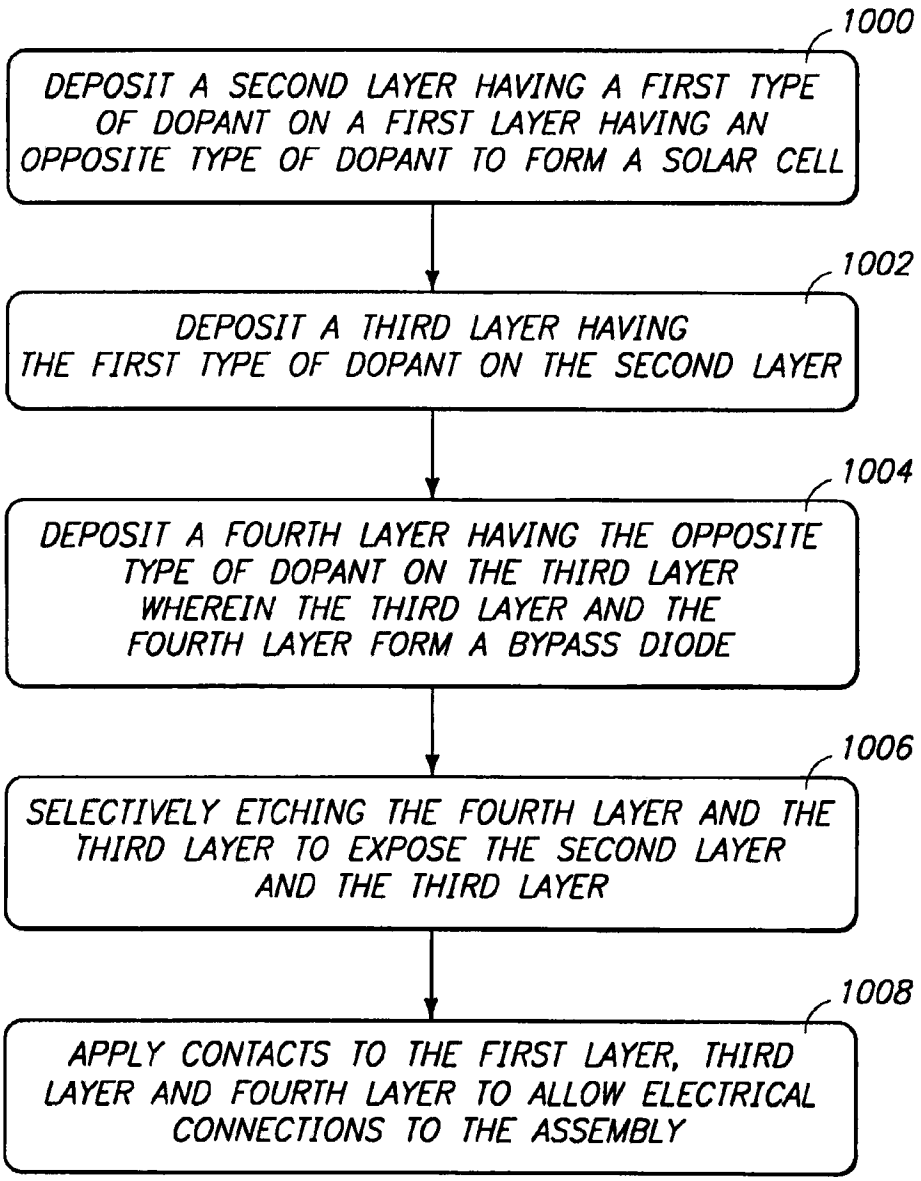

1000
DEPOSIT A SECOND LAYER HAVING A FIRST TYPE OF DOPANT ON A FIRST LAYER HAVING AN OPPOSITE TYPE OF DOPANT TO FORM A SOLAR CELL
1002
DEPOSIT A THIRD LAYER HAVING THE FIRST TYPE OF DOPANT ON THE SECOND LAYER
1004
DEPOSIT A FOURTH LAYER HAVING THE OPPOSITE TYPE OF DOPANT ON THE THIRD LAYER WHEREIN THE THIRD LAYER AND THE FOURTH LAYER FORM A BYPASS DIODE
1006
SELECTIVELY ETCHING THE FOURTH LAYER AND THE THIRD LAYER TO EXPOSE THE SECOND LAYER AND THE THIRD LAYER
1008
APPLY CONTACTS TO THE FIRST LAYER, THIRD LAYER AND FOURTH LAYER TO ALLOW ELECTRICAL CONNECTIONS TO THE ASSEMBLY

FIG. 10

INTERNATIONAL SEARCH REPORT

Inte. onal Application No
PCT/US 00/07403

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/142

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
PAJ, INSPEC, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 236 (E-428), 15 August 1986 (1986-08-15) -& JP 61 067968 A (SHARP CORP), 8 April 1986 (1986-04-08)	1-4
A	the whole document	5,7,11
X	US 4 997 491 A (HOKUYO SHIGERU ET AL) 5 March 1991 (1991-03-05)	1,3,7
Y	column 4, line 3 -column 5, line 63	8,10
A		5,11
Y	US 4 638 109 A (ISHIHARA TAKASHI ET AL) 20 January 1987 (1987-01-20)	8,10
A	column 3, line 33-56	6,13
	-/—	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 July 2000	19/07/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	van der Linden, J.E.

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter onal Application No
PCT/US 00/07403

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 535 614 A (SHARP KK) 7 April 1993 (1993-04-07)	1,3
A	column 8, line 13 -column 9, line 30	2,4,7,8
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 078 (E-1037), 22 February 1991 (1991-02-22) & JP 02 298080 A (SHARP CORP), 10 December 1990 (1990-12-10)	1
A	abstract	5,7,8
X	EP 0 369 666 A (MITSUBISHI ELECTRIC CORP) 23 May 1990 (1990-05-23)	1,3
A	column 7, line 22-54	5,7
A	PATENT ABSTRACTS OF JAPAN vol. 006, no. 218 (E-139), 2 November 1982 (1982-11-02) & JP 57 122580 A (IND SCIENCE & TECHNOL), 30 July 1982 (1982-07-30) abstract	1,2,7,8
P,X	WO 99 62125 A (TECSTAR POWER SYSTEMS INC) 2 December 1999 (1999-12-02) the whole document	1-14

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte .onal Application No
PCT/US 00/07403

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 61067968 A	08-04-1986	JP 1792870 C	14-10-1993
		JP 5001627 B	08-01-1993
US 4997491 A	05-03-1991	JP 2135786 A	24-05-1990
		DE 68917428 D	15-09-1994
		DE 68917428 T	22-12-1994
		DE 68923061 D	20-07-1995
		DE 68923061 T	09-11-1995
		EP 0369666 A	23-05-1990
		EP 0369717 A	23-05-1990
		US 5009720 A	23-04-1991
US 4638109 A	20-01-1987	JP 60240171 A	29-11-1985
		DE 3517414 A	21-11-1985
EP 0535614 A	07-04-1993	JP 2912496 B	28-06-1999
		JP 5160425 A	25-06-1993
		DE 69229030 D	02-06-1999
		DE 69229030 T	11-11-1999
		US 5330583 A	19-07-1994
JP 02298080 A	10-12-1990	NONE	
EP 0369666 A	23-05-1990	JP 3077382 A	02-04-1991
		JP 2135786 A	24-05-1990
		DE 68923061 D	20-07-1995
		DE 68923061 T	09-11-1995
		US 5009720 A	23-04-1991
		DE 68917428 D	15-09-1994
		DE 68917428 T	22-12-1994
		EP 0369717 A	23-05-1990
		US 4997491 A	05-03-1991
JP 57122580 A	30-07-1982	NONE	
WO 9962125 A	02-12-1999	AU 4193899 A	13-12-1999
		EP 1008188 A	14-06-2000